AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 2, 5 and 11-13 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a plurality of processors;

a trace circuit configured to present information at a port for debugging software in a selected processor of said processors;

a ~~connector~~ first circuit configured to (i) couple said trace circuit to said selected processor in response to a select signal, ~~and~~ (ii) transfer said information from said selected processor to said trace circuit while said selected processor is executing said software, (iii) transfer data from said trace circuit to said selected processor and (iv) present a first predetermined logic state to said processors other than said selected processor;

a second circuit configured to (i) transfer a first test data stream received by said selected processor to said trace circuit, (ii) transfer a second test data stream from said trace circuit to said selected processor and (iii) present a second predetermined logic state to said processors other than said selected processor; and

a boundary scan chain connected to each of said processors and said trace circuit.

2. (CANCELLED)

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~connector~~ second circuit is further configured to transfer ~~a~~ said first test data stream received by said selected processor through said boundary scan chain to said trace circuit.

4. (CURRENTLY AMENDED) The apparatus according to claim ~~3~~ 1, wherein said ~~connector~~ second circuit is further configured to transfer ~~a~~ said second test data stream from said trace circuit through said boundary scan chain to said selected processor.

5. (CANCELLED)

6. (CURRENTLY AMENDED) ~~The~~ An apparatus ~~according to claim 1, wherein said connector circuit comprises~~ comprising:

a plurality of processors;

a trace circuit configured to present information at a port for debugging software in a selected processor of said processors;

a first multiplexer configured to (i) couple said trace circuit to said selected processor in response to a select signal and (ii) multiplex said information from said processors to said trace circuit in response to said select signal while said selected processor is executing said software; ~~and~~

a first plurality of gates each coupled to one of said processors and configured to (i) transfer data selected by said select signal and (ii) present a first predetermined logic state while not selected by said select signal; and

a boundary scan chain connected to each of said processors and said trace circuit.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, ~~wherein said connector circuit further comprises~~ further comprising:

a second multiplexer configured to multiplex a plurality of first test data streams received by said processors to said trace circuit in response to said select signal; and

a second plurality of gates each coupled to one of said processors and configured to (i) transfer a second test data stream while selected by said select signal and (ii) present a second predetermined logic state while not selected by said select signal.

8. (ORIGINAL) The apparatus according to claim 6, wherein each of said gates comprises a logical AND gate having at least one input configured to receive said select signal.

9. (CURRENTLY AMENDED) A method for debugging software in a selected processor of a plurality of processors, comprising the steps of:

(A) coupling a trace circuit to said selected processor in response to a select signal;

(B) transferring information from said selected processor to said trace circuit while said selected processor is executing said software;

(C) presenting said information received by said trace circuit at a port; ~~and~~

(D) connecting said processors and said trace circuit through a boundary scan chain;

(E) transfer a first test data stream received by said selected processor to said trace circuit;

(F) transfer a second test data stream from said trace circuit to said selected processor; and

(G) presenting a first predetermined logic state to said processors other than said selected processor in response to transferring said second test data stream.

10. (ORIGINAL) The method according to claim 9, further comprising the steps of transferring data from said trace circuit to said selected processor.

11. (CANCELLED)

12. (CANCELLED)

13. (CANCELLED)

14. (CURRENTLY AMENDED) The method according to claim ~~13~~ 9, further comprising the step of presenting a second predetermined logic state to said processors other than said selected processor in response to transferring said second test data stream.

15. (CURRENTLY AMENDED) The method according to claim ~~12~~ 9, wherein said step of transferring said information comprises the sub-step of multiplexing said information in response to said select signal.

16. (CURRENTLY AMENDED) The method according to claim ~~15~~ 9, wherein said step of transferring said second test data stream comprises the sub-step of gating said second test data stream in response to said select signal.

17. (CURRENTLY AMENDED) The method according to claim ~~16~~ 9, wherein said step of transferring said first test data stream comprises the sub-step of multiplexing said first test data stream in response to said select signal.

18. (ORIGINAL) The method according to claim 17, wherein said step of transferring said second test data stream comprises the sub-step of gating said second test data stream in response to said select signal.

19. (CURRENTLY AMENDED) An apparatus comprising:

means for coupling a trace circuit to a selected processor of a plurality of processors in response to a select signal;

means for transferring information from said selected processor to said trace circuit while said selected processor is executing software;

means for presenting said information received by said trace circuit at a port; ~~and~~

boundary scan means connected to said processors and said trace circuit;

means for transfer a first test data stream received by said selected processor to said trace circuit;

means for transfer a second test data stream from said trace circuit to said selected processor; and

means for presenting a predetermined logic state to said processors other than said selected processor in response to transferring said second test data stream.

20. (CURRENTLY AMENDED) The circuit according to claim 1, wherein said processors, said trace circuit, said first circuit and said ~~connector~~ second circuit are embedded in a single integrated circuit.